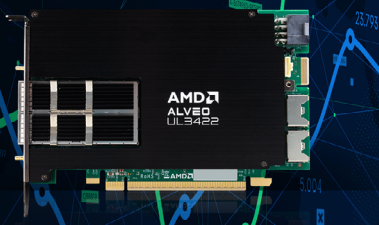
AMD ALVEO™ UL3422 FPGA ACCELERATOR CARD

FOR ULTRA-LOW LATENCY TRADING IN A SLIM FORM FACTOR FOR BROAD MARKET DEPLOYMENT

AMD
together we advance_



OVERVIEW

Today's leading proprietary trading firms, market makers, hedge funds, brokerages, and exchanges are continually seeking new ways to enhance tick-to-trade performance for a competitive edge.

The AMD Alveo™ UL3422 FPGA accelerator card combines ultra-low latency networking with adaptable hardware, accelerating trading strategies at nanosecond speeds. Powered by the AMD Virtex™ UltraScale+™ VU2P FPGA, the Alveo UL3422 card features a latency-optimized transceiver technology for the world's fastest trade execution and tick-to-trade latency of network I/O.[1]

Its slim, FHHL form factor provides the flexibility to deploy across a breadth of server configurations, and as an FPGA-based trading card, supports traditional hardware design tools, development frameworks, and ecosystem IP.

KEY APPLICATIONS

TARGET USERS

- Proprietary Traders
- Market Makers
- Hedge Funds
- Brokerages
- Exchanges
- Market Data Feed Vendors

USE CASES

- Ultra-Low Latency Trading
- Pre-Trade Risk Analysis
- Market Data Delivery & Distribution

HIGHLIGHTS

PURPOSE-BUILT FOR ULTRA-LOW LATENCY (ULL) PERFORMANCE

- Custom FPGA device and new transceiver architecture for fast trade execution
- Less than 3 ns transceiver latency & up to 7X performance vs. previous generation[2]

SLIM FORM FACTOR FOR COST-EFFECTIVE DEPLOYMENT

- FHHL form factor to fit in a breadth of server configurations
- Optimized for rack-space, compute density, and power efficiency

EASE OF DEVELOPMENT FOR FAST PATH TO TRADE

- Traditional FPGA flows through AMD Vivado™ tool with reference designs
- Open-source PyTorch development flow for AI-enabled trading algorithms
- IP and trading development frameworks from ecosystem partners

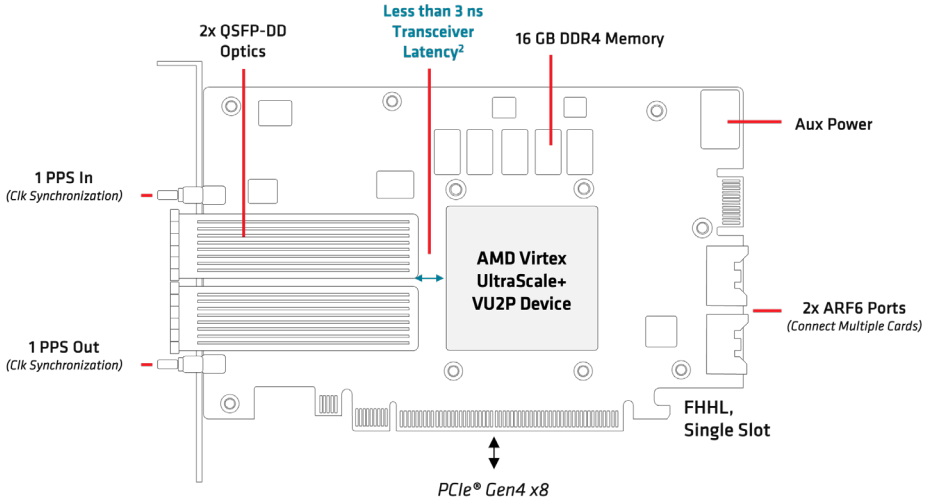
Less than 3 ns transceiver latency[2]

PURPOSE-BUILT FOR ULTRA-LOW LATENCY PERFORMANCE

The AMD Alveo UL3422 accelerator card features a purpose-built Virtex™ UltraScale+ FPGA device with a new transceiver architecture. The FPGA fabric is capable of 644 MHz clock speeds at 16-bit operation for streaming market data. The device also integrates hardened Ethernet MAC and PCS IP for ultra-low latency data transmission and control management, simplifying timing closure for ULL trading. With two network ports supporting 10 Gb/s and 25 Gb/s data rates, the FPGA and transceiver architecture meets the operational standards of most market exchanges.

ALVEO™ UL3422 ACCELERATOR CARD

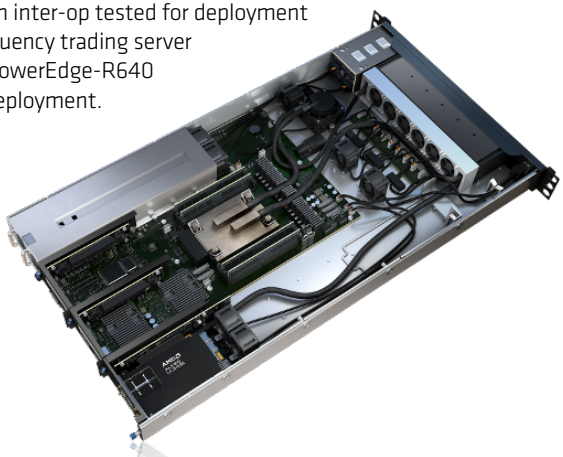
Powered by Purpose-Built FPGA with Ultra-Low Latency Transceiver Architecture



SLIM FORM FACTOR FOR COST-EFFECTIVE DEPLOYMENT

With a small, efficient design, the Alveo™ UL3422 FinTech accelerator streamlines the number of network ports, onboard memory, and board-to-board connectivity options compared to its predecessor—the Alveo UL3524 accelerator card—for cost-effective server deployment. Its compactness enables optimized rack space, compute density, and power consumption to limit infrastructure and co-location expenses.

The Alveo UL3422 accelerator has been inter-op tested for deployment in the 1U Orion HF X410R-G6 high-frequency trading server from Hypertec, as well as the 1U Dell PowerEdge-R640 server, both available for immediate deployment.



EASE OF DEVELOPMENT FOR FAST PATH TO TRADE

The Alveo UL3422 FinTech accelerator supports traditional FPGA development workflows for a fast path to profitable trading. The card is supported by the AMD Vivado™ Design Suite for RTL development, coupled with reference designs for rapid evaluation of latency performance. The nxFramwork from Exegy delivers a hardware and software environment with pre-built infrastructure IP for seamless integration of user algorithms into complete trading engines, order execution systems, pre-trade risk check gateways, or custom applications.

With the increasing adoption of AI in algorithmic trading, AMD Research Labs provides the open-source FINN development framework. Using quantization techniques, FINN enables developers to reduce the size of their AI models, compile to hardware, and integrate into a trading algorithm's datapath for low-latency performance. For pre-built AI solutions, Xelera Technologies offers Xelera Silva low-latency machine learning IP—complete with software stack, API support, and example design.

AMD Vivado

exegy

XELERA SILVA

SPECIFICATIONS

AMD ALVEO UL3422

CARD FEATURES AND SPECIFICATIONS	
FPGA RESOURCES	• 787K look-up tables (LUTs) | 1,722K registers • 1,680 DSP slices • 256 Mb embedded memory (76 Mb block RAM, 180 Mb UltraRAM)
TRANSCEIVERS	• 8 GTYP transceivers (32.75 Gb/s) | 32 GTF ultra-low latency transceivers (25.78 Gb/s)
ONBOARD MEMORY	• 16 GB DDR4, 64b +8b ECC at 2400 MT/s
INTERFACES	• 2x QSFP-DD (16x10/25G ports)
EXPANSION PORTS	• Two ARF6 supports additional 16x10/25G ports to connect multiple cards • One Pico-Clasp connector for sideband
CLOCK SYNCHRONIZATION	• 1 PPS In, 1PPS Out
CONFIGURATION AND DEBUG	• 2 Gb QSPI, JTAG over Micro USB
PCIE® INTERFACE	• PCIe Gen4 x8 (x16 physical connector)
FORM FACTOR	• Full-height, half-length (FHHL) | Single slot
POWER AND THERMAL	• 180W electrical | 120W TDP | Passive cooling
PRODUCT SKU	• A-UL3422-P16G-PQ-G

TAKE THE NEXT STEP

- For pricing and availability, contact your local sales representative or complete the Alveo™ UL3422 Inquiry Form.
- To request software licensing and technical documentation, visit the Alveo UL3422 Secure-Site Request Form.

ENDNOTES

1. The 2024 AMD world record for latency is based on 3rd party testing commissioned by AMD and Exegy, by Strategic Technology Analysis Center, LLC (STAC®) in April 2024, using the STAC-T0 benchmark to test the AMD Alveo UL3524 accelerator card powered by the AMD Virtex Ultrascale+ VU2P FPGA, running on the Exegy nxFramework and Exegy nxTCP-UDP-10g-ULL IP Core, in a Dell PowerEdge R7525 server with AMD EPYC 7313 processors. See https://stacresearch.com/news/AMD240422 for the full STAC report. AMD holds the previous world record for latency (2020): https://www.stacresearch.com/news/XLX200514. Stated results for the Alveo UL3524 accelerator have been extrapolated to the AMD Alveo UL3422 card, based on identical silicon and product features. (ALV-20).

2. Based on a simulated comparison by AMD using the Synopsis VCS 2019.06-SP2 ultra-low latency Virtex UltraScale+ VU2P GTF transceivers and GTY transceivers in February 2022 (ALV-15).

DISCLAIMERS

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